

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of:

Riichiro TAKEMURA et al.

Appln. No.:

Filed: Herewith

For: SEMICONDUCTOR DEVICE

(Continuation of Appln. No. 10/251,772 filed September 23,
2002)

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

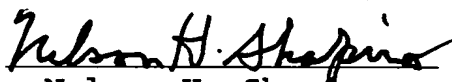
Sir:

Applicants wish to make record the documents cited in
prior Application Nos. 10/347,804 filed January 22, 2003,
10/251,772 filed September 23, 2002, and 09/914,028 filed
August 22, 2001, whether cited by Applicants or by the
Patent Office. The documents are listed on the attached
Form-1449.

Respectfully submitted,

NHS:lmb

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October 27, 2003

By: 
Nelson H. Shapiro
Reg. No. 17,095

FORM PTO-1449				Atty. Docket No. XA-9530D		Appln. No.	
<u>LIST OF DOCUMENTS CITED BY APPLICANT</u>				Applicant Riichiro TAKEMURA et al.			
				Filing Date Herewith		Group	
U.S. PATENT DOCUMENTS							
Examiner Initial		Document Number	Date	Name	Class	Sub-class	Filing Date
	AA	5,412,605	5/2/95	OOISHI	365	203	
	AB	5,375,095	12/20/94	YAMADA et al.	365	230	
	AC	6,014,337	1/11/00	MAKINO	365	205	
	AD	5,900,665	5/4/99	TOBITA	257	357	
	AE	5,867,440	2/2/99	HIDAKA	365	226	
	AF	5,801,576	9/1/98	OOISHI	327	530	
	AG	5,325,336	6/28/94	TOMISHIMA et al.	365	207	
	AH	6,097,623	8/00	Sakata et al.	365	207	
	AI	5,949,729	9/99	Suyama et al.	365	207	
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FOREIGN PATENT DOCUMENTS							
Examiner Initial		Document Number	Date	Country	Class	Sub-class	Translation
	AL	6-309872	11/4/94	JAPAN			Abstract
	AM	63-211191	9/2/88	JAPAN			Abstract
	AN	WO97/24729	7/10/97	JAPAN			Abstract
	AO	2000-58785	2/25/00	JAPAN			Abstract
	AP	11-297071	10/29/99	JAPAN			Abstract
	AQ	4-212454	8/4/92	JAPAN			Abstract
OTHER (including author, title, date, pertinent pages, etc.)							
	AR	K. Ito, Baihuukan, VLSI Memory, 1 st issue, November 5, 1994, pp. 161-167					
	AS	Yamada et al., "A 64Mb Dram With Meshed Power Line and Distributed Sense-Amplifier Driver," ISSCC91 Digest of Technical Papers, 1991, pp. 108-109					
	AT	Hidaka, "A 34-ns 16-Mb DRAM with Controllable Voltage Down-Converter," IEEE Journal of Solid State Circuits, Vol. 27, No. 7, 1982, pp 1020-1027					
Examiner				Date Considered			
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.							

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				Filing Date Herewith		Group	
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Examiner Initial		Document Number	Date	Country	Class	Sub-class	Translation
	AL*	10-269772	10/9/98	JAPAN			Abstract
	AM*	11-149768	6/2/99	JAPAN			Abstract
	AN*	10-275466	10/13/98	JAPAN			Abstract
	AO*	9-55482	2/25/97	JAPAN			Abstract
	AP*	8-138381	5/31/96	JAPAN			Abstract
	AQ*	5-62461	3/12/93	JAPAN			Abstract
OTHER (including author, title, date, pertinent pages, etc.)							
	AR*	Eto et al., "A 1Gb SDRAM with Ground Level Precharged Bitline and Non-Boosted 2.1V Word Line," ISSCC98 Digest of Technical Papers, 1998, pp. 82-83					
	AS*						
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Examiner				Date Considered			
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				TAKEMURA et al.			
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FOREIGN PATENT DOCUMENTS							
Examiner Initial		Document Number	Date	Country	Class	Sub-class	Translation
	AL'	9-204777	8/5/97	JAPAN			Abstract
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	AN'						
	AO'						
	AP'						
	AQ'						
OTHER (including author, title, date, pertinent pages, etc.)							
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	AS						
	AT						
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